# EXHIBIT 11

#### UNITED STATES PATENT AND TRADEMARK OFFICE

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#### BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 9,318,160

Issued: April 19, 2016

Filed: July 21, 2014

Inventor: Hyun Lee

Title: Memory Package with Optimized Driver Load and Method of Operation

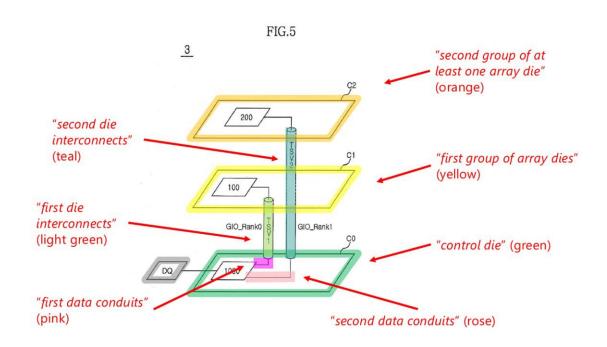
Inter Partes Review No. IPR2023-00883

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PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,318,160

Petition for *Inter Partes* Review of U.S. Patent No. 9,318,160 an arrangement, each die interconnect has a respective "data conduit[]" for transferring the corresponding data signal.

EX1003, ¶237.

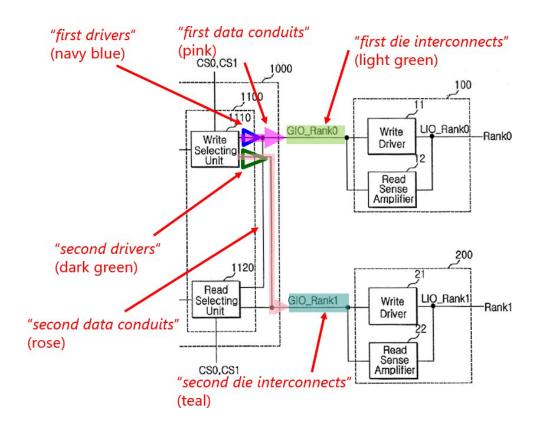


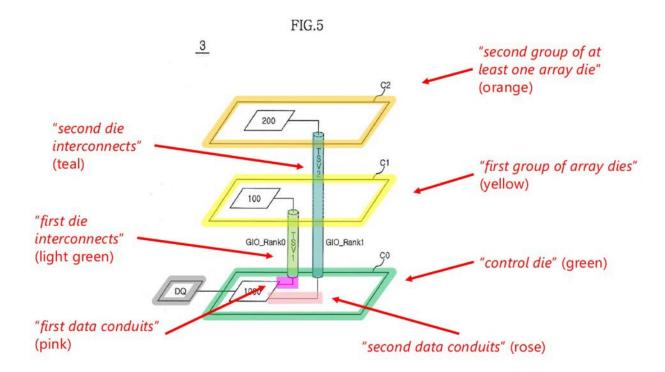
## g) [1.e.4]-[1.e.5] First and Second Drivers

Ground 1 teaches "the first data conduit[s] [(pink)] including first drivers [(navy blue)] each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies," and "the second data conduit[s] [(rose)] including second drivers [(dark green)] each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size

[larger dark green triangle, given the longer TSV2] being different from the first driver size [smaller navy blue triangle, given the shorter TSV1]." EX1014, Figs. 3, 5 (below); EX1003, ¶252-266. The claim limitations "the first data conduit" and "the second data conduit" lack proper antecedent basis given that [1.e.2]-[1.e.3] recite "first data conduits" and "second data conduits."

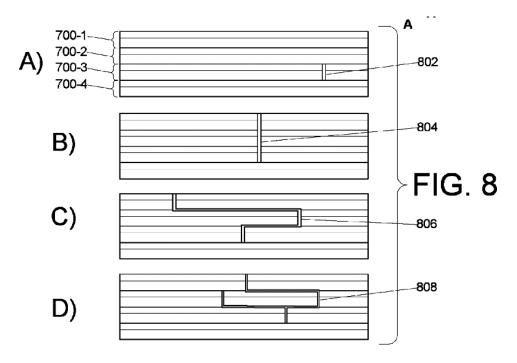
EX1003, ¶253. Nevertheless, it would be obvious in light of Ground 1 that each "data conduit" could include one or more "drivers," as explained further below, thus rendering the claimed "data conduit[s]" obvious either way despite the lack of proper antecedent basis. *Id*.





Given that <u>Kim</u> expressly illustrates in Figure 5 (above) that the first die interconnects, like TSV1, are shorter than the second die interconnects, like TSV2, a POSITA would have been motivated by <u>Wyman</u> (in the combination of Ground 1, pp.32-34) to use drivers of different strengths (i.e., "first drivers" having a "first driver size" and "second drivers" having a "second driver size") for <u>Kim</u>'s different sized TSV1 and TSV2. EX1003, ¶257-265. As discussed above, <u>Wyman</u> teaches that shorter paths (e.g., 802 below, like TSV1 above) have less load and thus require less drive, while longer paths (e.g., 804 below, like TSV2 above) have more load and thus require a larger drive, motivating a POSITA to drive the shorter TSV1 with a smaller drive, and the longer TSV2 with a larger drive, to use power in an efficient manner, but without using the full strength of a driver, which Wyman teaches would be "wasteful and inefficient." EX1017, 1:22-

24, 2:61-65, 6:15-30, 6:44-50, Figs. 7, 8 (below); EX1003, ¶¶257-265; *see also supra* pp.6-8 and EX1030, pp.135-138 (disclosing different-sized transistors to achieve different driver strengths).



For example, <u>Wyman</u> discloses circuitry that includes one or more drivers (502-1 to 502-4, below) that are selectively activated to achieve the optimal driving strength for a given signal. EX1017, 5:11-14 ("a designer may now utilize and tapoff at five locations (506-1, 506-2, 506-3, 506-4, 508 [below]) depending on the drive requirements for a specific element or device"), 7:14-18 (describing modifying the output drive current to meet the requirements of a particular output load), Fig.5 (below), Figs.10-11; *see also supra* pp.6-8; EX1003, ¶260.

### IX. CONCLUSION

Petitioners therefore respectfully request that Trial be instituted and that claims 1-20 be canceled as unpatentable.

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